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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,033	SMAUS ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed on June 16th, 2006.

Title

3. Objection is withdrawn.

Specification

4. Objection is withdrawn.

Claim Objections

1. Objections are withdrawn.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7-8, 13-15, 17, 18 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Mendelson et al. (U.S. Publication No. US 2002/0095553) hereinafter referred to as Mendelson.

7. As per claim 1, Mendelson discloses a microprocessor, comprising:

an instruction cache; (Fig. 3 L2 cache 340) *The examiner asserts that the L2 cache stores instructions.*

a trace cache; (Fig. 3 FTC 320 and MTC 330)

and a prefetch unit coupled to the instruction cache and the trace cache; (Fig. 3 Cache Manager 310) *The examiner asserts that the management logic fetches instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330.*

wherein the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache. (Paragraph 39, lines 3-6).

Mendelson also discloses the prefetch unit configured to fetch instruction code from a system memory for storage within the instruction cache (Paragraph 39, lines 3-6)

Examiner asserts that the trace information located within FTC 320 and MTC 330 includes instruction code. Examiner also asserts that the FTC and MTC are considered to be system memory note the following definition from the American Heritage Dictionary, 4th addition:

Memory: Also called computer memory, storage.

a) the capacity of a computer to store information subject to recall.

b) the components of the computer in which such information is stored.

By this definition, the FTC and MTC are clearly system memory. Consequently, Mendelson discloses a prefetch unit (Cache Manager) configured to fetch instruction code (trace information) from a system memory (FTC or MTC) for storage within the instruction cache (L2 cache).

8. As per claim 7, Mendelson discloses the microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the evicted trace is predicted unlikely to re-execute. (Paragraph 40 lines 5-7) *The examiner asserts that Mendelson's use counter is a method of indicating if a trace is likely to be re-used.*

9. As per claim 8, Mendelson discloses a computer system, comprising:

a system memory; (Fig. 1A memory 132)

and a microprocessor coupled to the system memory, comprising:

an instruction cache; (Fig. 3 L2 cache 340) *The examiner asserts that the L2 cache stores instructions.*

a trace cache; (Fig. 3 FTC 320 and MTC 330)

and a prefetch unit coupled to the instruction cache and the trace cache; (Fig. 3 Cache Manager 310) *The examiner asserts that the management logic fetches*

instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330.

wherein the prefetch unit is configured to fetch a line of instnlctions into the instruction cache in response to a trace being evicted from the trace cache. (Paragraph 39, lines 3-6).

Mendelson also discloses the prefetch unit configured to fetch instruction code from a system memory for storage within the instruction cache (Paragraph 39, lines 3-6)

10. As per claim 13, Mendelson discloses a computer system containing the processor of claim 6, hence claim 13 is rejected under the same grounds as claim 6 above.

11. As per claim 14, Mendelson discloses a computer system containing the processor of claim 7, hence claim 14 is rejected under the same grounds as claim 7 above.

12. As per claim 15, Mendelson discloses a method, comprising:

evicting a trace from a trace cache; (Paragraph 39, lines 3-6).

fetching a line of instructions into an instruction cache in response to said evicting. (Paragraph 39, lines 3-6).

13. As per claim 17, Mendelson discloses a method performing the function of the processor of claim 6, hence claim 17 is rejected under the same grounds as claim 6 above.

14. As per claim 18, Mendelson discloses a method performing the function of the processor of claim 7, hence claim 18 is rejected under the same grounds as claim 7 above.

15. As per claim 23, Mendelson discloses a microprocessor performing the function of the processor of claim 1, hence claim 23 is rejected under the same grounds as claim 1 above.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2-6, 9-12, 16, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mendelson.

18. As per claim 2, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to fetch a line into instruction cache

comprising instructions that correspond to operations that precede a branch in the evicted trace.

19. Official notice is taken that traces may consist of multiple branch instructions. If a trace has two ore more branch instructions in it, it is guaranteed to have at least one instruction which precedes a branch instruction.

20. Traces with multiple branch instructions are beneficial when branch prediction logic can unroll multiple loops into a single string of instructions. They provide faster processing by providing instructions which are likely to execute to the execution logic of the processor.

21. It would have been obvious to one of ordinary skill in the art at the time of invention to have included traces including multiple branch instructions in those stored in Mendelson's trace cache for the benefit of faster execution.

22. As per claim 3, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions that correspond to operations that follow a branch in the evicted trace.

23. Official notice is taken that traces may consist of multiple branch instructions. If a trace has two ore more branch instructions in it, it is guaranteed to have at least one instruction which follows a branch instruction.

24. Traces with multiple branch instructions are beneficial when branch prediction logic can unroll multiple loops into a single string of instructions. They provide faster

processing by providing instructions which are likely to execute to the execution logic of the processor.

25. It would have been obvious to one of ordinary skill in the art at the time of invention to have included traces including multiple branch instructions in those stored in Mendelson's trace cache for the benefit of faster execution.

26. As per claim 4, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache.

27. Official notice is taken that traces commonly consist of multiple lines when stored in a cache.

28. Multiple-line traces encompass multiple instructions likely to execute in sequence. Instructions strung together across multiple lines provide more sequential instructions that a single line can provide. This provides the execution logic with a more steady stream of instructions, allowing faster processing.

29. It would have been obvious to one of ordinary skill in the art at the time of invention to have included multiple-line trace cache entries in Mendelson's invention for the benefit of faster processing.

30. When a multiple-line trace is evicted from the trace cache, it is fetched by the L2 cache, as described in paragraph 39.

31. As per claim 5, Mendelson discloses the microprocessor of claim 4, wherein the prefetch unit is configured to fetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace. *The examiner asserts that no matter what number of branch operations are included in an evicted trace, the number of lines fetched by the L2 cache is in some proportion to that number.*

32. As per claim 6, Mendelson discloses the microprocessor of claim 1.

Mendelson fails to disclose a cache that checks for duplicate information within the cache to inhibit the storing said duplicate information.

Examiner asserts that it would have been obvious at the time of the invention for one of ordinary skill in the art to take the invention of Mendelson and utilize a cache system that, when presented with information to store, checks if that information already exists and inhibits duplicate storage. In particular, within the invention of Mendelson, the combination would check when there is an eviction from the trace cache.

Regarding the motivation, Examiner asserts that this technique is extremely common practice within cache systems. Storing the same information within a waste of resources that can create a detriment to the processing system with regards to space, cost, power, and often speed.

33. As per claim 9, Mendelson discloses a computer system containing the processor of claim 2, hence claim 9 is rejected under the same grounds as claim 2 above.

34. As per claim 10, Mendelson discloses a computer system containing the processor of claim 3, hence claim 10 is rejected under the same grounds as claim 3 above.

35. As per claim 11, Mendelson discloses a computer system containing the processor of claim 4, hence claim 11 is rejected under the same grounds as claim 4 above.

36. As per claim 12, Mendelson discloses a computer system containing the processor of claim 5, hence claim 12 is rejected under the same grounds as claim 5 above.

37. As per claim 16, Mendelson discloses the method of claim 15, further comprising checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace. See claim 6.

38. As per claim 19, Mendelson discloses a method performing the function of the processor of claim 2, hence claim 19 is rejected under the same grounds as claim 2 above.

39. As per claim 20, Mendelson discloses a method performing the function of the processor of claim 3, hence claim 20 is rejected under the same grounds as claim 3 above.

40. As per claim 21, Mendelson discloses a method performing the function of the processor of claim 4, hence claim 21 is rejected under the same grounds as claim 4 above.

41. As per claim 22, Mendelson discloses a method performing the function of the processor of claim 5, hence claim 22 is rejected under the same grounds as claim 5 above.

Response to Arguments

2. Applicant's arguments, see below, filed 16 June 2006, with respect to claims 6 and 16 have been fully considered and are persuasive. The rejection of claims 6 and 16 have been withdrawn.

3. Applicant's arguments filed 16 June 2006 with regards to the remaining claims have been fully considered but they are not persuasive.

Applicant states:

"The Examiner submits that a new title is required that is clearly indicative of the invention to which the claims are directed. However, the current title, "Instruction Cache Prefetch Based on Trace Cache Eviction", is clearly indicative of the claimed invention."

Examiner agrees. Objection is withdrawn.

4. Applicant states:

"First, the Examiner asserts that the L2 cache of Mendelson stores instructions and is, thus, analogous to the instruction cache of Applicants' claim 1. However, L2 cache 340 of Mendelson is a second-level trace cache, that may be added to trace cache subsystem 120, and that is distinguished from a traditional L2 cache in that the L2 trace-cache 340 is not an instruction cache, as would be understood by one of ordinary skill in the art, but a trace cache."

Examiner asserts that the L2 cache 340 does include instructions and the anticipation of Applicant's instruction cache, as claimed, is perfectly reasonable.

5. Applicant states:

"The Examiner further submits that the Cache Manager 310 of Mendelson is analogous to Applicants' prefetch unit. Applicants assert, however, that Cache Manager 310 is clearly not the same as the prefetch unit of Applicants' claim 1. First, the Cache Manager is clearly not configured to fetch instruction code from a system memory for storage within the instruction cache, as recited in claim 1. Furthermore, a prefetch unit, such as that of Applicants' claim 1, is well-known in the microprocessor art and one of ordinary skill in the art at the time the invention was made would not consider Cache Manager 310 of Mendelson to be a prefetch unit."

Examiner disagrees. Regarding point 1) the Cache Manger is configured to fetch instruction code from a system memory for storage within the instruction cache (L2 cache). Regarding point 2) Examiner asserts that the Cache Manager completes all the functionality of the prefetch unit required by the claim; therefore, it is reasonable to

consider it part of the prefetch unit. The elements of an actual CPU are not always as concrete as the conceptual tools used to analyze them. Components interact in such a complex way that the separation of different components is entirely up to the person analyzing the invention and not the invention itself.

6. Applicant states:

"The Examiner submits that L2 cache 340, Cache Manager 310, and paragraph [0039] of Mendelson disclose wherein the prefetch unit as configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache. The Examiner asserts, 'the management logic fetches instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330.' While this paragraph does describe that traces evict from FTC 320 or MTC 330 are transferred for storage in the L2 trace cache (under control of Cache Manager 310), this has nothing to do with a prefetch unit fetching a line of instructions into the instruction cache in response to a trace being evicted from the trace cache."

Examiner disagrees. The confusion in the argument above appears to ignore the components of Mendelson used to anticipate claim 1. Since Applicant's instruction cache is anticipated by Mendelson's L2 cache 340 and Applicant's prefetch unit is anticipated by Mendelson's Cache Manager, it follows that a prefetch unit fetches a line of instructions into the instruction cache in response to a trace being evicted from the trace cache."

7. Applicant states:

"Regarding claim 6, contrary to the Examiner's assertion, Mendelson fails to teach or suggest the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache. The Examiner asserts that if an instruction trace is already stored in the L2 cache, it cannot be evicted from the trace cache, and hence, will not be refetched by the L2 cache. However, claim 6 recites what the prefetch unit is configured to do in response to the eviction of certain traces. Therefore, the Examiner's remarks about what happens when a trace in Mendelson is not evicted do not apply to claim 6."

Examiner agrees. The rejection is now an obvious rejection under 35 USC 103.

8. Applicant states:

"Regarding claim 16, contrary to the Examiner's assertion, Mendelson fails to teach or suggest checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace. The Examiner asserts that the processor must inherently check if a trace is already stored in the L2 cache before storing it and that storing the same trace cache more than once in the L2 cache is a waste of resources. Applicants respectfully disagree. First, Applicants' claim does not recite checking a trace cache (such as Mendelson's L2) for lines of instructions comprising the instructions corresponding to the evicted trace, but instead recites checking the instruction cache (Mendelson's cache memory 140)."

Examiner agrees. This aspect is not inherent. The rejection has been changed to an obvious rejection under 35 USC 103.

9. The arguments made with regard to claims 2, 3, 4, 7 and 15 all seem to ignore the analogous nature of the instruction cache (as claimed) and the L2 cache (as disclosed by Mendelson). Examiner asserts that if that fact is considered, the remaining limitations fall into place and are adequately described within the original rejection.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Peled et al. (U.S. Patent No. 6,216,206) discloses a dedicated trace victim cache to store evicted traces for future reuse.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made.

The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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